Claims 2 and 9 stand rejected under 35 U.S.C. Section 103(a) as unpatentable over Purcell et al. and Normile et al. and further in view of Harney et al.

The claims have been amended, and it is respectfully submitted that the claims distinguish over the references, even in combination, for the reasons set forth below. Therefore, it is requested that the rejection be reconsidered and withdrawn.

In accordance with this invention as stated beginning at page 3, line 22 of the specification:

> Thus in this environment use of a dedicated fully functional MPEG decompression integrated circuit is not necessary, and instead a substantial portion of the decompression can be off-loaded onto other conventional computer system elements. Thus only a relatively small portion of the actual data decompression must be performed by dedicated circuitry, if any. In accordance with the invention, the MPEG decompression task is allocated amongst various already existing elements of a typical computer system and if necessary, depending on the capabilities of these other elements, an additional relatively small (hence inexpensive) dedicated MPEG decompression circuit is provided.

> Thus advantageously in accordance with the present invention, the MPEG (compressed using layers) content of data is decompressed in a computer system typically already including a microprocessor, graphics accelerator, frame buffer, peripheral bus and system memory. A shared computational approach between the microprocessor (host processor), graphics accelerator and a dedicated device makes best use of the computer system existing resources. This is a significant advantage over the prior art where the MPEG decompression is performed entirely by a dedicated processor. (Emphasis added.)

The MPEG standard referred to herein and described on page 1 of the present specification is the established (published) MPEG 1 and 2 standards. These define the data structure discussed at page 2 of this specification and shown in Figure 1, including the upper white/green book layer, the system layer, and the lower level video and audio layers.

Further, the present specification discusses the known C-Cube Microsystems' commercially available MPEG decompression chips (see specification at page 2, beginning at line 32):

> In these products the MPEG audio and visual decompression (of all layers) is accomplished completely and dedicated circuitry in an internally programmable microcontroller. ... Thus <u>these chips accomplish the entire decompression on their own,</u> ...
> (Emphasis added.)

The first reference Purcell et al. is of this type. Purcell, et al., discloses at column 6, lines 4 and following:

> Fig. 2 shows an embodiment of the present invention in the video decompression circuit 200. This embodiment of the present invention is provided in the CL950 MPEG Video Decompression Process (<u>the "CL950 chip"</u>), available from C-Cube Microsystems, San Jose, CA.

Therefore, Purcell et al. discloses dedicated single chip MPEG decompression. While Purcell et al. discloses a connection to a host bus in Figure 2, it is made clear (see column 6, lines 34 to 48) that this is for purposes of "data input and output" (lines 40-44) rather than for actual decompression processing. Thus no processing takes place in the host for decompression purposes because it is entirely accomplished within the single chip 200 depicted in Purcell et al., Figure 2.

Additionally, and as implied by the Examiner, Purcell et al. does not disclose <u>any</u> decompression of a "system layer". This is because the MPEG "standard" described by Purcell et al. is a <u>draft</u> MPEG "standard" as indicated at the bottom of column 30 of Purcell et al. by the label "Draft". This is dated 9/14/90, years before the actual MPEG 1 standard was published in 1993. Apparently, this <u>draft</u> version of MPEG did not include anything higher than the video or audio layers; see the associated table of contents at columns 28-30 of Purcell et al., in which the highest MPEG layer is the "Video Sequence" layer at pages 4 and 8. In

this draft MPEG "standard", there was no book or system layer, i.e. higher level layers, to be decompressed at all.

The second reference Normile et al. similarly does not appear particularly pertinent. While Normile et al. does show a host computer, for instance in Figure 4, there is no indication that this host computer performs any actual decompression tasks. Instead, the host computer only provides the transfer of data to/from the <u>dedicated</u> decompression processor 400 shown in Normile et al. Figure 4. See Normile et al. column 9, beginning at line 22:

> Referring to FIG. 4, an architecture of a parallel processing system which is used for compression/decompression of moving video images in the preferred embodiment is shown as 400. ... Although host processor 410, in the preferred embodiment, is typically the bus master of system bus 425, at certain times display controller 426 assumes control of system bus 425.

Thus, it is clear that the host computer does not perform any decompression, but instead is the bus master for purposes of input/output and does not even function all the time as the bus master, being supplanted at times by the display controller. This of course is because the host computer's role is so limited, i.e. only to data control purposes, rather any actual decompression.

Hence Claim 1 distinguishes over the references, singly or in combination. Claim 1 as amended recites "the computer system including a <u>host processor located on a first integrated circuit chip</u> connected via peripheral bus to <u>a secondary processor located on a second integrated circuit chip</u>" (Emphasis added.) This makes clear the partitioning in accordance with this invention, as illustrated for instance in Figure 2. Advantageously in accordance with this invention, the existing general purpose microprocessor in a computer system is used for data decompression, in conjunction with a secondary processor (which may be dedicated to data decompression or not). Clearly, this distinguishes over Purcell et al. and Normile et al.,

which both disclose a single chip dedicated MPEG decompression circuit, for achieving entire decompression without any decompression tasks being undertaken by a separate processor chip.

Moreover, the particular partitioning of tasks in accordance with Claim 1 is not suggested by any of the references. Claim 1 also recites "decompressing at least a system layer, which is a higher level layer than a video layer, of the compressed data in the host processor; and decompressing other layers of the set of predetermined layers including the video layer, in the secondary processor." Again, advantageously in accordance with Claim 1, the tasks most suitable for the host processor are performed by it, while the more intensive computational tasks are undertaken by the secondary processor (which may be dedicated).

As discussed above, Purcell et al. does not even mention the possibility of higher level MPEG layers (above the video layer); instead, Purcell et al. only discloses decompression of the video layer itself. Apparently at the time of Purcell et al. there was no higher level layer in the MPEG "standard." The Examiner stated the "host processor taught by Normile et al. processes at least a system layer of compressed data. That is, the host processor reads and determines one complete frame of compressed data from a disk or memory and transfers the data to the coprocessors ...". However, it is not believed this is a fair reading of Claim 1, which is explicit about "a system layer, which is a higher level layer than a video layer". Normile et al. is merely handling data I/O through its host. Normile et al. is not at all explicit about any MPEG (or other decompression standard) and does not disclose a "higher level layer" as recited in Claim 1. Hence, Claim 1 distinguishes over the references, alone or in combination, for these reasons and is allowable.

Claims 2-7, dependent upon Claim 1, distinguish over the references for at least the same reasons as does Claim 1.

Claim 3 has been amended to further define "the host processor". Advantageously in accordance with Claim 1, there is an actual decompression step taking place in a host microprocessor; neither Normile et al. nor Purcell et al. disclose such a step, and hence, Claim 3 distinguishes thereover for this additional reason.

System Claim 8 has been amended to recite additional features similar to those of Claim 1, and hence Claim 8 distinguishes over the references for reasons similar to those as discussed above in conjunction with Claim 1.

Claims 9-15, dependent upon Claim 8, distinguish over the references for at least the same reason as does the base claim.

Claim 10 has been amended to recite additional features similar to those of Claim 3, and hence additionally distinguishes over the references and is allowable.

Claims 1-15 are provisionally rejected under 35 U.S.C. §101 as claiming the same invention as Claim 1-15 of copending application S.N. 08/489,488. This rejection is overcome since independent Claims 1 and 8 as amended are not identical to the claims in copending S.N. 08/488,489. A Terminal Disclaimer is submitted herewith to overcome any obviousness-type double patenting rejection contemplated by the Examiner, with regard to S.N. 08/488,489.

Claims 15-26 are provisionally rejected under 35 U.S.C. §102(e) as anticipated by copending application S.N. 08/488/489.

The §102(e) rejection is traversed; the present disclosure is not identical to that of S.N. 08/489,488, but includes Figs. 10-13 (and the accompanying portions of the specification) directed to the frame reconstruction circuit. This disclosure is not a part of S.N. 08/488,489. Hence the §102(e) rejection is not well founded, and its withdrawal is requested.

Therefore, it is respectfully submitted that all pending Claims 1-26 are allowable, and allowance is requested. If the Examiner contemplates other action, the Examiner is requested to call the undersigned at 408/453-9200.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231,
on _Nov. 6, 1997_ , 19__.
Norm Klivan   _Nov 6, 1997_
Attorney for Applicant(s)   Date of Signature

Respectfully submitted,

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